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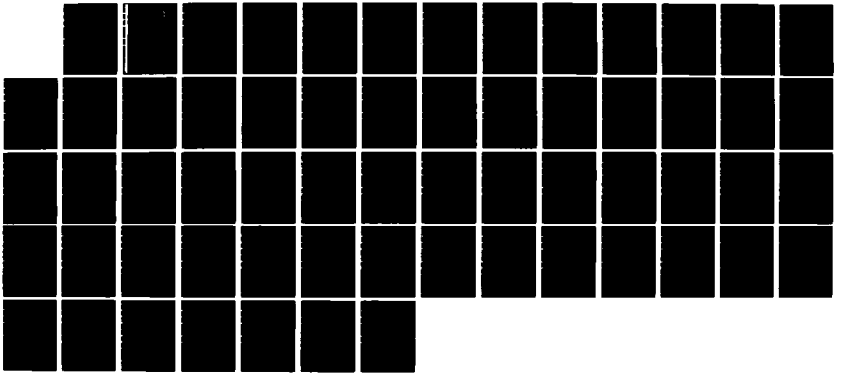

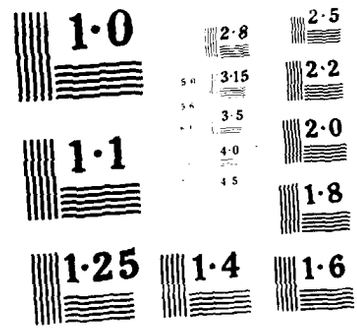
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LARGE SIGNAL MODELING AND ANALYSIS OF THE GaAs MESFET

TECHNICAL REPORT NO. 86-P-2

Vincent D. Hwang and Tatsuo Itoh

June 1, 1986

U.S. Army Research office
Contract NO. DAAG29-84-K-0076

University of Texas
Electrical Engineering Research Laboratory
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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: ARO 21438.27-EL	2. GOVT ACCESSION NO.: N/A
3. RECIPIENT'S CATALOG NUMBER: N/A	
4. TITLE (and Subtitle): Large Signal Modeling and Analysis of the GaAs MESFET	5. TYPE OF REPORT & PERIOD COVERED: Technical Report, 6/1/86
	6. PERFORMING ORG. REPORT NUMBER: 86-P-2
7. AUTHOR(s): Vincent D. Hwang and Tatsuo Itoh	8. CONTRACT OR GRANT NUMBER(s): DAAG29-84-K-0076
9. PERFORMING ORGANIZATION NAME AND ADDRESS: University of Texas, Austin, TX 78712	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: U. S. Army Research Office, Post Office Box 12211, Research Triangle Park, NC 27709	12. REPORT DATE: 7/9/86
	13. NUMBER OF PAGES: 56
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

NA

18. SUPPLEMENTARY NOTES

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19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

GaAs MESFET
Large signal model
Multiple reflection technique

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The purpose of this work is to develop a large signal lumped circuit model of the GaAs MESFET to aid in the designs of microwave MESFET circuits. The circuit elements of this model are obtained either directly or indirectly from the DC and RF measurements of the device to be modeled.

To analyze this circuit model, a nonlinear circuit simulation computer program is written. This routine is base on a hybrid time-frequency domain iterative algorithm called 'multiple reflection technique.' To improve the

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20. Abstract (continued)

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The validity of the analysis algorithm is first checked by comparing the simulation results of a MESFET with published data. The large signal model developed is then confirmed by comparing the simulation results of a MESFET modeled in this work to the experimental results.

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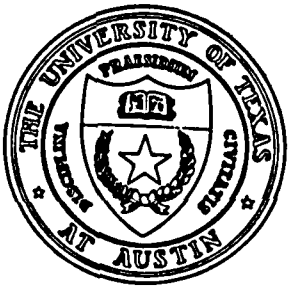

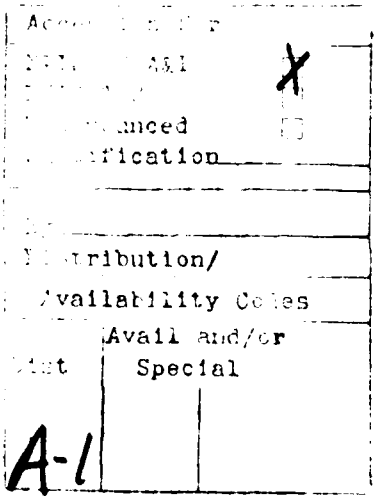

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Large Signal Modeling and Analysis of GaAs MESFET

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Chapter 1 Introduction

The GaAs metal semiconductor field effect transistor has become the workhorse device in the microwave industry. The device is used extensively in many small-signal applications such as low noise amplifier. Due to the exceptional power performance of the GaAs MESFET, which is comparable or superior to most other commercial microwave solid-state devices, a wide range of power applications have been seen. The applications of the GaAs MESFET such as for power amplifiers, oscillators and mixers are growing rapidly.

Despite the large demands for GaAs MESFET as power devices, the large-signal design techniques for these circuits are still relatively primitive. This situation can be explained by two reasons: 1. the immaturity of the GaAs technology in general, 2. The difficulty in characterizing the device in microwave and millimeter wave frequencies. Conventionally, GaAs MESFET power amplifiers and oscillators are designed by using small-signal S-parameters with tweaking and tuning of the circuit coming later. In power amplifier designs, the load-pull method can also be used to determine the optimum load impedance. However, this load-pull procedure is laborious and cannot predict the gain performance of the circuit.

A large signal model of the GaAs MESFET can aid in the design of a nonlinear MESFET circuit tremendously. Several research

efforts have tried to develop a numerical model of the GaAs MESFET[1][2][3]. These numerical models use numerical techniques such as a finite element method to solve the nonlinear differential equations that govern the device's physical properties. These numerical models are helpful in understanding device operation and can be used to aid in the design of the MESFET. However, they are impractical for circuit level design purposes due to the long computation time required for these models. Madjar and Rosenbaum[4], Shur[5], Chua and Sing[6] developed approximate analytical models for the GaAs MESFET. With the exception of Madjar and Rosenbaum's model, none of these analytical models have shown validity in large signal circuit design. Furthermore, this type of model requires the detailed knowledge of the device's physical parameters which often cannot be obtained accurately. Willing, Raucher, and de Santis[7] developed a circuit model of the GaAs MESFET by measuring the device S-parameters at various bias points. The data collected is then used to extract linear element values of the circuit model. The voltage dependencies of the nonlinear elements are obtained by using a polynomial curve-fitting to the S-parameters measured at each bias point. Although this approach was shown accurate, it has the drawback of being very tedious. Tajima, et al.[8][9], Materka and Kacprzak[10] used a quasi-static approach to develop their circuit model. In this approach, the voltage dependencies of nonlinear elements are assumed to be the same as in the DC condition. They used DC current-voltage characteristics of the

MESFET to establish the voltage dependencies of the nonlinear elements and used S-parameter optimization to obtain linear element values. Their results showed this approach is accurate at least up to 18 GHZ. In this study, a crcuit model similar to the one used by Materka and Kacprzak is employed. A systematic, yet simple technique of identifying circuit element and circuit parameter values is developed.

The circuit model thus developed needs to be analyzed by a nonlinear circuit analysis technique. Frequently used nonlinear circuit analysis methods can be divided into two classes: 1. the time domain analysis, 2. the hybrid analysis that iterates between frequency domain and time domain.

The time domain approachs includes the direct integration method and the shooting method. The direct integration method is a brute force method which solves the nonlinear differential equations that describes the nonlinear circuit at each discretized time step until it reaches steady state. This approach often requires long computation time if the transient time is long. To avoid long transient analysis, Colon and Trick[11] proposed a shooting method that uses Newton's iteration algorithm to find a steady state solution. Skelboe[12] used a different kind of shooting method with an extrapolation algorithm. Even with the shooting method, The computation time for the time domain approach is long compared with a hybrid type of analysis.

Nakhla and Vlach used a hybrid analysis called 'harmonic

balance method'. In this algorithm, the circuit under analysis is decomposed into two parts, the nonlinear subnetwork and the linear subnetwork. The linear subnetwork is described by linear equations in the frequency domain and the nonlinear network is described by nonlinear differential equations in the time domain. Interconnecting the linear and nonlinear network can be achieved by relating the time and frequency domain by the Fourier transformation. The harmonic compoments of voltages an/or currents at the interconnection of the linear and nonlinear subnetworks are chosen as an independent variable of the system. These variables are optimized by an iterative algorithm, so that the linear equations of the linear network and the nonlinear differential equation of the nonlinear network are all satisfied. With a suitable optimizing method, the harmonic balance method can be quite efficient. However, the success of this approach often depends on good initial guess values of the voltage and/or current harmonic components. If the initial guess values are not close enough to the actual solution, the solution might converge to local minimums or not converge at all.

Kerr[14], proposed a different kind of hybrid technique which is called the 'multiple reflection method' This method also iterates between the time and frequency domain. It requires no initial guess. However, the speed of convergence is relatively slow. In the present work, the multiple reflection technique is modified by adding a 'voltage update algorithm'. For MESFET circuit analsyis, the modified multiple reflection method is found to be much more

efficient than the original multiple reflection method.

Chapter 2 of this thesis describes the GaAs MESFET model. The large signal model is evolved from the conventional small signal lumped circuit model. From an initial sensitivity study, some of the circuit elements are identified as nonlinear elements. By means of the quasi-static approach, these elements are modeled by nonlinear equations. The linear element values are obtained from DC and RF measurements.

Chapter 3 is devoted to the large signal curcuit analysis techniques. The multiple reflection method is introduced first. In this method, the FET circuit is divided into a nonlinear part and linear part. The solution is arrived at by solving the nonlinear and linear circuit iteratively. A voltage update procedure is then added to the multiple reflection method to increase convergence speed.

Chapter 4 presents the simulated results and the experimental data. The validity of the modified multiple reflection method is first confirmed by comparing the data obtained with Materka's MESFET circuit simulations. An arbitrarily chosen device is modeled using the techniques in chapter 2. Simulated results and measured data of this device are compared.

Chapter 5 forms the conclusion and suggests future research paths. Possible related future research topics can be the modeling of a dual gate MESFET, the analysis of other large signal devices such as FET mixer, FET oscillator and FET multiplier.

Chapter 2 GaAs MESFET Modeling

The purpose of this research is to develop a practical model of the GaAs MESFET to aid in the large signal GaAs MESFET circuit design. This model must meet four requirements:

1. The modeling technique should be general, so that it applies to devices with various dimensions and physical parameters.
2. The procedures of extracting circuit parameters should be reasonably simple.
3. The model can be analyzed in a computationally efficient manner.
4. The model should be reasonably accurate in predicting device performance.

2.1 The large signal equivalent circuit

The large-signal equivalent circuit is derived from the conventional small-signal equivalent circuit. Figure 2.1 is such a small-signal equivalent circuit. The position of each lumped element in an actual device is illustrated in figure 2.2. L_d, L_g and L_s are the bound wire inductances. R_g is the metallization resistance at gate. R_d and R_s consist of the ohmic contact resistances and the resistances in the active layer. R_i is the charging resistance to the gate-source capacitance. C_{ds} is the capacitance that exists in the

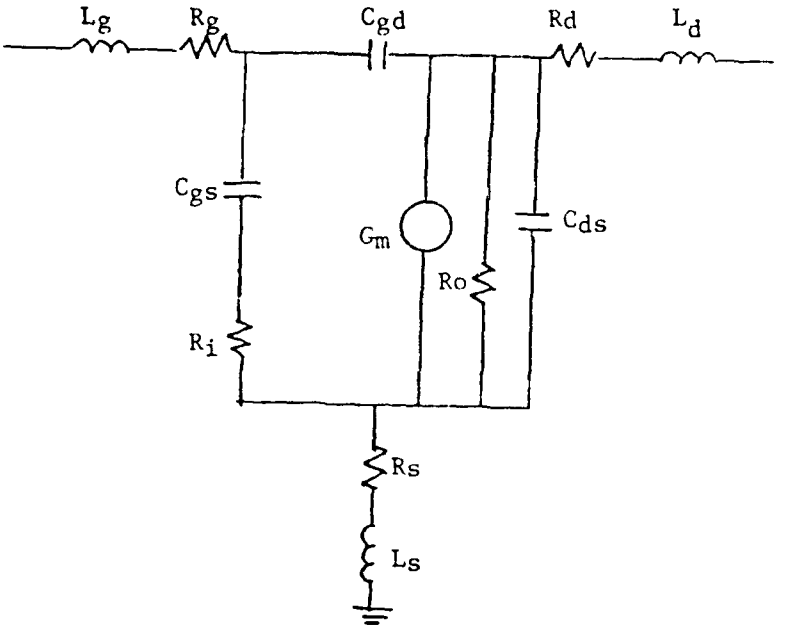


Figure 2.1 Small signal equivalent circuit of MESFET

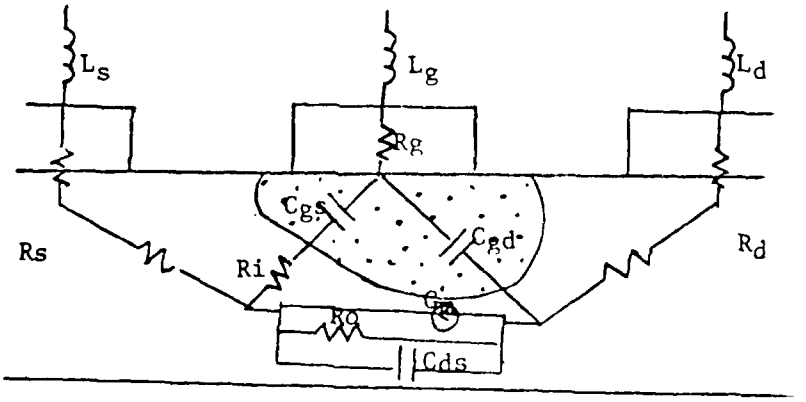


Figure 2.2 Location of small-signal equivalent circuit elements

channel region. R_0 is the output resistance. Precisely speaking, all these elements exhibit certain degrees of nonlinearity. By measuring the S-parameters of the device at sufficiently different bias points, and curve-fitting the small signal equvalent circuit to the S-paramenters measured at each bias point, the element values of the small-signal equvalent circuit versus bias voltages curve can be established. It was found that L_s, L_g, L_d, R_d, R_s, R_g and R_i do not exhibit strong bias dependency[7]. These elements are considered as linear elements in this study. At this point, a priliminary large signal equivalent circuit can be drawn(fig. 2.3). Notice that R_0 and G_m are combined to a single nonlinear element $I_{ch}(Vg, Vd)$. Taking into account gate voltage swing to positive voltage and the drain break-down phenomenon, forward gate bias current I_f and drain to gate current I_{br} are added to form the final large signal equivalent circuit(fig. 2.4).

2.2 Extracting linear element values

R_g, R_d, R_s, L_g, L_d and L_s are identified as linear elements. Their values are assumed to be voltage independent. In general, these elements have small values and are difficult if not impossible to measure directly. Often, these values are established by measuring device S-parameters at certain bias conditions and curve-fitting the small-signal equvalent circuit to the S-parameters.

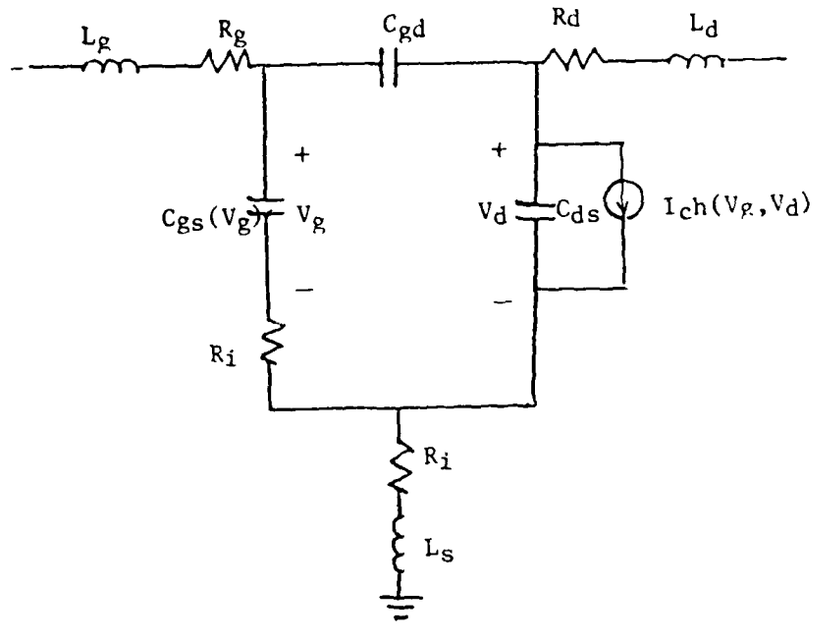


Figure 2.3 Priliminary large-signal equivalent circuit

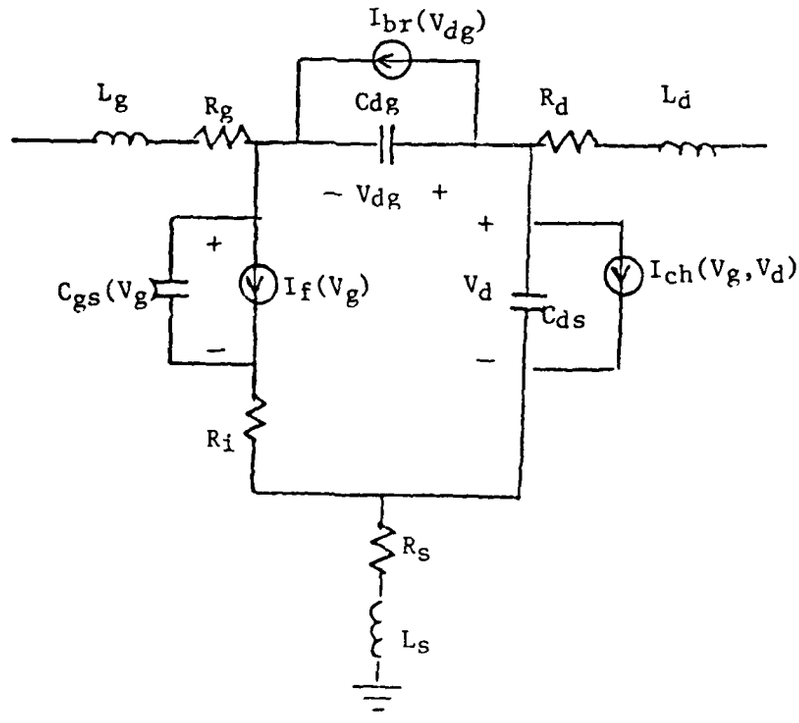


Figure 2.4 Final large-signal equivalent circuit

As Diamond and Laviron[15] have suggested, the S-parameter measurements of a device at V_{DS}= 0. V, permits a more accurate evaluation of device parasitics because the device can be represented by a simpler equivalent circuit. Figure 2.5 is the equivalent circuit at V_{DS} =0. The channel region under the gate is depleted evenly due to the lack of drain bias voltage. This depleted channel region is modeled by the distributed R-C network in the equivalent curcuit. Curtice and Camisa[16] found that when trying to optimize the circuit element values of figure 2.5 to curve fit the measured S-Parameters at V_{DS}=0, with small difference in the error function, the optimum values of R_g, R_s and R_d vary widely depending upon the optimization method and the initial guess values. This suggests the parastic resistance values R_g, R_d and R_s obtained in this way may not be reliable. In this work, a DC measurement technique called Fukui's method[17] will be used to determine parasitic resistance values. The unknown element values of figure 2.5 are now reduced to 6(R, C,C_{ds}, L_g, L_d and L_s). Now, the bound wire inductance values L_g, L_d and L_s can be optimized with greater accuracy.

A Hughes' PF-6000 GaAs MESFET is chosen to be analyzed. The device has a gate length of 0.6μm and a gate width of 960 μm. The following procedure are taken to evaluate the linear element values.

Since the parasitic resistance values are small (on the

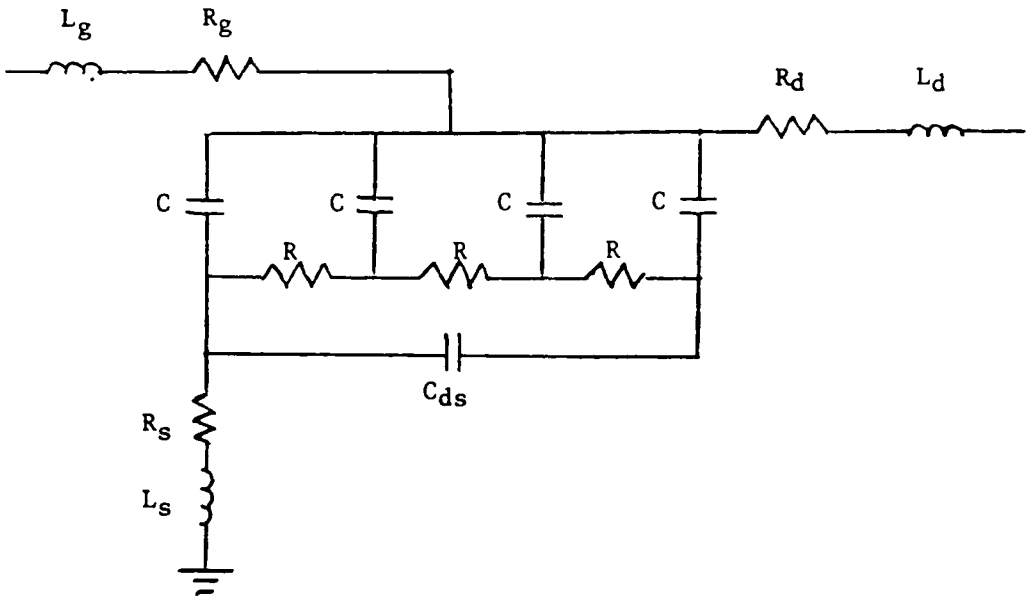


Figure 2.5 MESFET equivalent circuit at V_{DS}=0

order of 1 ohm), the measurement system needs to be carefully calibrated. The Rg+Rs value can be approximated by measuring the slope of V_{gs} vs. I_{gs} at high current level with the drain at ground and the source open. Similarly, R_d+R_g can be calculated(fig. 2.6). The R_d+R_s value is extrapolated by the following steps:

a. measuring the drain I-V curve in the linear region (figure 2.7).

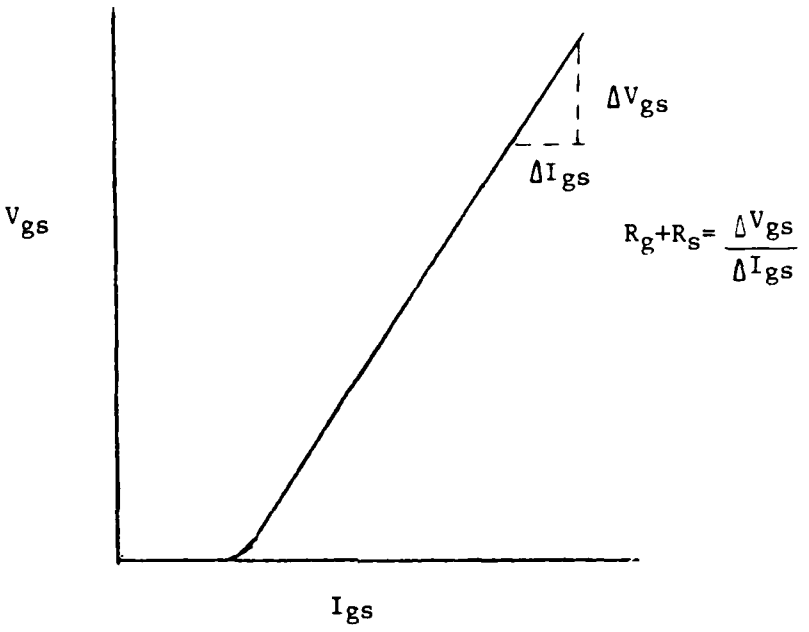
b. plotting the slope of V_{DS}/I_{DS} at each gate bias voltage vs. X, where X is defined as,

$$X=\{1-SQRT[(V_b-V_{gs})/(V_p+V_b)]\}^{-1} \qquad (2.1)$$

V_b is the built-in voltage for the Schottky-gate and V_p is the pinch-off voltage.

The linear extrapolation of this curve to the Y axis gives the value of R_s+R_d (figure 2.8). From the values of R_s+R_d, R_g+R_s and R_d+R_g, the values of R_g, R_d and R_s can be subsquently calculated.

With R_d, R_s and R_g known, L_s, L_d and L_g can be optimized to the S-parameters measured. This is conveniently done by using Super-Compact[18].



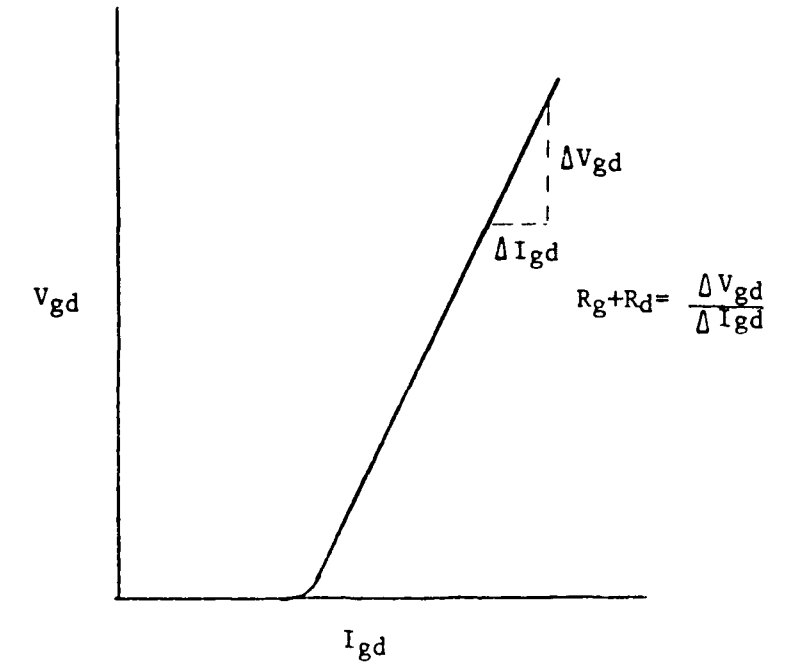


Figure 2.6 Determination of R_g+R_S and R_g+R_d

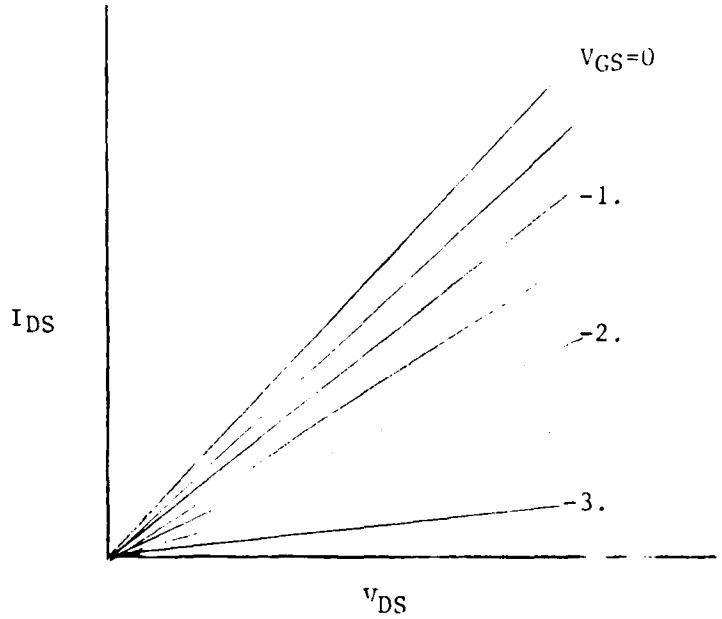


Figure 2.7 I-V curve in the linear region

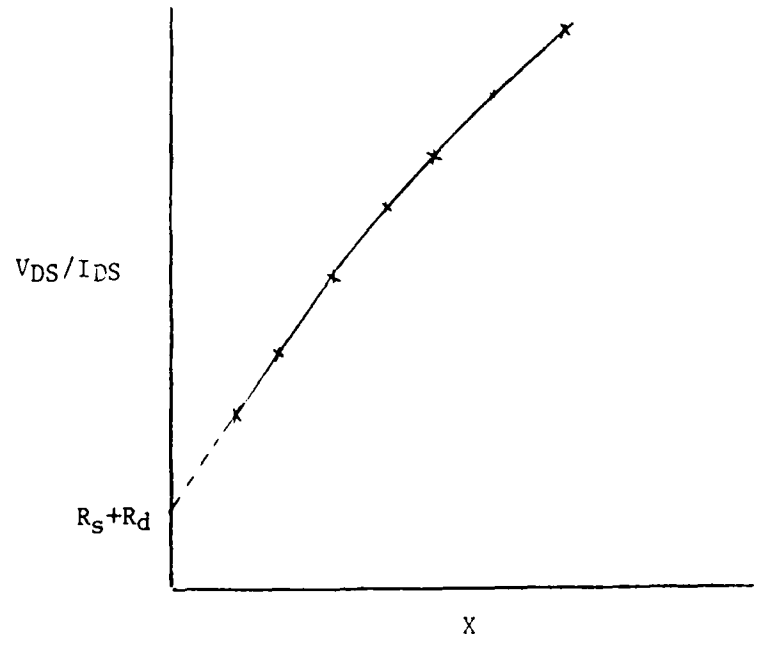


Figure 2.8 Extrapolation of R_d+R_S

2.3 Modeling of nonlinear elements

Nonlinear elements are the ones that exhibit bias voltage dependent values. The quasi-static approach is taken to model the nonlinear elements. In this approach, the assumption is made that the voltage dependency of the nonlinear element at high frequency can be determined from its dependency on DC bias voltage.

a. Channel current and breakdown current

The nonlinear expression for channel current and drain to gate breakdown current are determined by the DC drain current versus the drain and gate bias voltages curves. Figure 2.9 is the measured curve of the Hughes PF-6000 FET. The drain current is equal to the sum of the channel current and the breakdown current,

$$I_{ds}=I_{ch}+I_{br} \qquad (2.2)$$

The breakdown current I_{br} is significant only at high V_{ds} and high V_{gs} values, where the drain to gate voltage V_{dg} is high. The negative differential rsistance observed at high gate voltage after saturation is due to the Gunn-domain effect which is caused by the velocity saturation characteristics of GaAs[19]. The Gunn-domain effect produces a dipole layer in the active layer near the drain side of the gate. This dipole layer also produces capacitance effects and will be discussed later. This negative resistance phenomenon is especially

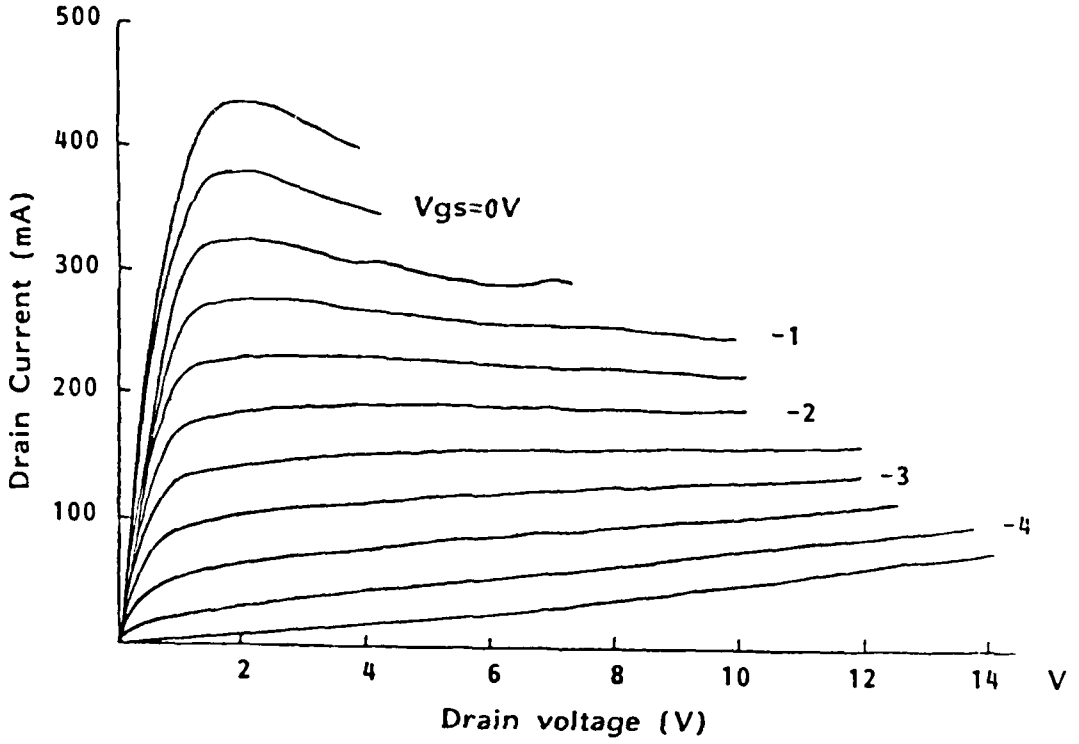


Fig. 2.9 Measured I-V curve of Hughes PF-6000 MESFET

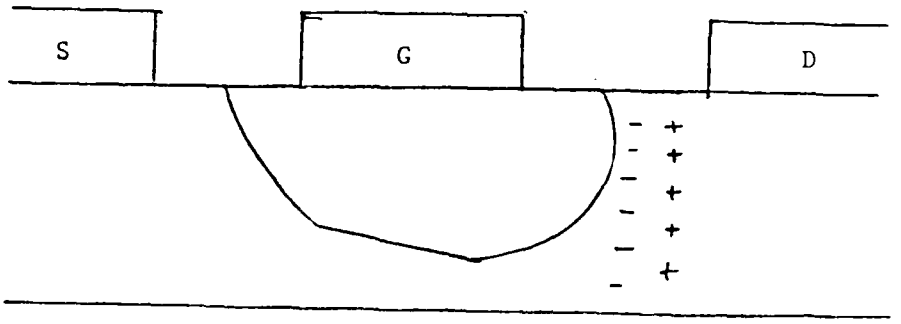


Figure 2.10 Location of the dipole layer

pronounced in a short channel GaAs FET, as in the case of a microwave GaAs FET. In short channel devices, a high electric field region exists in the channel. Electrons that enter this high field region are accelerated to a velocity as high as twice the equilibrium velocity before they relax to the equilibrium velocity[20]. This velocity overshoot shifts the dipole layer into a gap between the gate and drain. Figure 2.10 shows the location of this dipole layer.

the emperical expression proposed by Materka[10] is modified to model the channel current I_{ch},

$$I_{ch}=I_{dss} \times (1-V_g(t-\tau)/V_p)^2 \times \tanh[cV_d/(V_g(t-\tau)-V_p)] \qquad V_d \le V_{sat}$$

$$=I_{dss} \times (1-V_g(t-\tau)/V_p)^2 \times \tanh[cV_d/(V_g(t-\tau)-V_p)] - V_d \times g_o/(V_s-V_g(t-\tau))^q \qquad V_d > V_{sat} \tag{2.3}$$

$$\text{where } V_p = V_{po} + \gamma V_d$$

The breakdown current is modeled by an exponential expression,

$$I_{br}=I_{sr} \exp(\beta V_{dg}) \tag{2.4}$$

It should be noted that even though the expression for I_{br} is similar to the one of diode forward current, they represent different physical phenomenons. The parameters I_{dss}, c, g_o, V_{po}, γ, V_s, V_{sat}, I_{sr} and β

are optimized to the measured I-V curves. Using these two emperical expression, the simulated I-V curves for the PF-6000 MESFET is shown in figure 2.11. The parameter τ in (2.3) is the propagation delay time due to the finite velocity of the charge carriers which travel in the channel region. Electrons entering the channel at the source end travel for a time τ before it reaches the drain end. This propagation delay time is a basic limitation of the device. Typically, τ is on the order of 10ps. At low operating frequencies, τ can be neglected. As frequencies get higher, τ becomes an increasingly important factor. To calculate τ, the velocity destribution $U(x)$ of carriers along the channel region needs to be known, and

$$\tau = \int_{s}^{D} 1/U(x)\, dx \qquad (2.5)$$

Since $U(x)$ is bias dependent, τ is also bias dependent. Due to the high field effect, the velocity distribution $U(x)$ cannot be easily calculated. For simplicity, τ is assummed constant in this study. This approximation should be reasonable in the saturation region of the I-V curves where the charge carriers travel at the saturation velocity in most of the channel region. This constant value of τ can be conveniently obtained by using the small-signal equivalent circuit of the MESFET in the Super-Compact, which has a time delay option. In

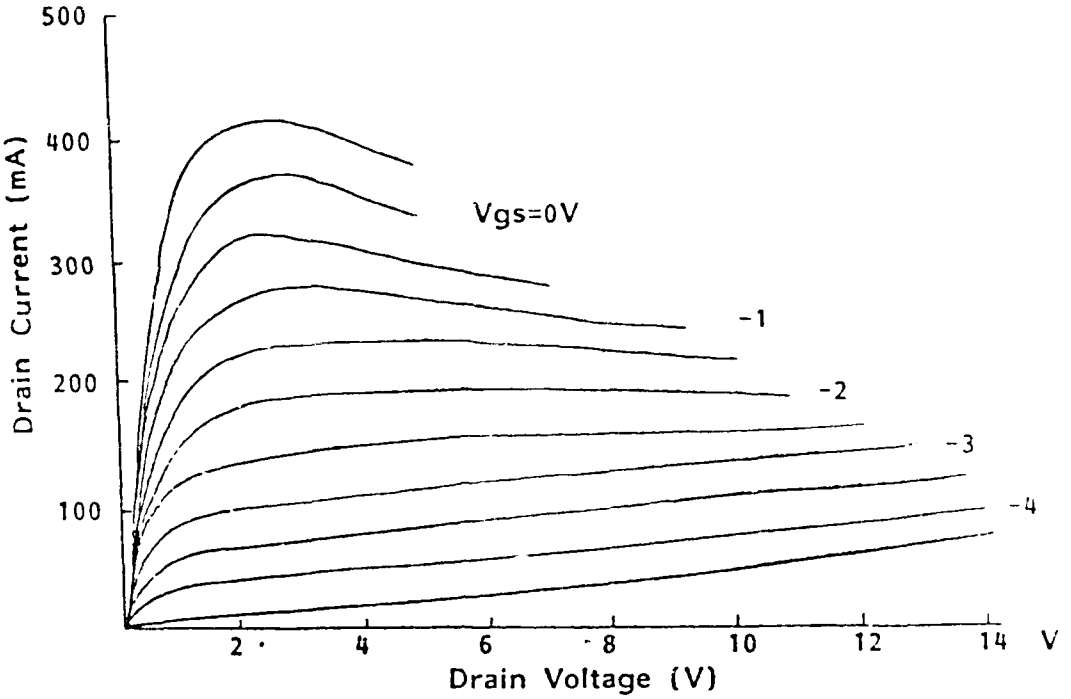


Figure 2.11 Simulated I-V curve of PF-6000 MESFET

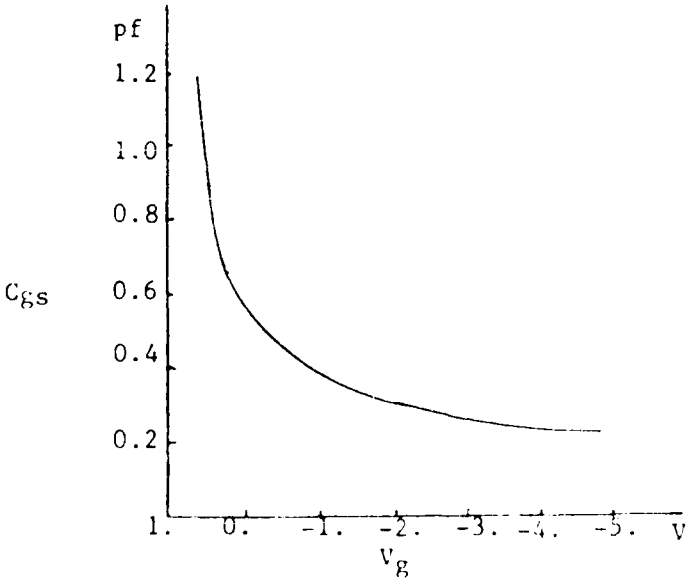


Figure 2.12 voltage dependence of C_{gs}

this equivalent circuit, the value of τ is optimized to fit measured S-parameter values at a normaly biased condition (eg. V_{GS}=-2.V, V_{DS}=7V for the PF-6000 MESFET).

b. Forward gate-bias current

The forward gate bias current is modeled by the diode forward bias current,

$$I_f = I_{so} \exp(\alpha V_g) \qquad (2.6)$$

I_{so} and α can be obtained by measuring I_f versus V_{gs} with the drain terminal open ,and plotting I_f vs. Vg on log paper, where

$$V_g = V_{gs} - I_f(R_s + R_g) \qquad (2.7)$$

The slope of this curve equals α, and the intercept on the Y-axis equals I_{so}.

c. Gate to source and gate to drain capacitances

The gate to source capacitance C_{gs} consists of 2 components:

$$C_{gs} = C_{sp} + C_{sd} \qquad (2.8)$$

C_{sp} is the capacitance due to gate and source contact metalization. C_{sd} is the gate to source depletion capacitance. Similarly, C_{gd}-the gate to drain capacitance is expressed as

$$C_{gd}=C_{dp}+C_{dd} \qquad (2.9)$$

C_{dp} is the capactance due to gate and drain contact metalization. C_{dd} is the gate to drain depletion capacitance. C_{sd} and C_{dd} together contribute to the total gate depletion capacitance. Willing, et al., have shown that C_{gs} and C_{gd} are both gate voltage and drain voltage dependent[7], with C_{gs} being weakly drain voltage dependent. To model C_{gs}, the depletion capacitance C_{sd} is assumed to be gate voltage dependent only and is represented by the Schottky diode depletion capacitance expression,

$$C_{sd}(V_g)=C_{so}/\mathrm{SQRT}(1-V_g/V_b) \quad \text{for } V_g \leq .8V_b \qquad (2.10)$$

where V_b is the build-in voltage of the Schottky barrier. For $V_g > .8V_b$, the charge storage capacitance is assumed to dominate and increases linearly with V_g with its slope equal to the slope at $V_g=.8V_b$. The metalization capacitance is constant and can be calculated by using the closed form formula for coupled microstrip lines[21]. Now, the total expression for Cgs can be represented as

$$C_{gs}=C_{so}/\mathrm{SQRT}(1-V_g/V_b)+C_{sp} \quad \text{,for } V_g < .8V_b \qquad (2.11)$$

$$=2.236C_{so}+5.59C_{so}/V_b \times (V_g-.8Vb)+C_{sp} \quad \text{, for } V_g > .8V_b$$

Figure 2.12 shows this gate voltage dependence of C_{gs}.

The gate to drain cpapcitance C_{gd} decreases rapidly as V_d increases in the linear region of the I-V curves. After saturation,

the shape of the depletion region under the gate at the drain side does not change much with an increase in drain voltage and the depletion capacitance C_{dd} becomes small. In this model, C_{dd} is assumed to decrease linearly to 0. at the saturation voltage V_{sat}. The gate voltage dependence of C_{dd} is the same as that of C_{sd} in this region. The total gate to drain capacitance C_{gd} is

$$C_{gd}=C_{go}/SQRT(1-V_g/V_b)\ X\ (1-V_d/V_{sat})+ C_{dp} \quad , \text{for } V_d \leq V_{sat}$$

$$=C_{dp} \quad , \text{for } V_d > V_{sat} \qquad (2.12)$$

C_{dp} the metallization capacitance can be calculated again by closed form expression for coupled microstrip lines. The curve for C_{gd} is shown in figure 2.13. C_{go} of (2.12) and C_{so} of (2.11) can be obtained by drawing the device equivalent circuit at a zero biased condition as shown in figure 2.14, and by using the S-parameters measured at this bias condition to optimize C_{go} and C_{so} values.

d. R_i and C_{ds}

R_i is the gate to source capacitance charging resistance. The product of R_i and C_{gs} is the gate to source capacitance charging time constant. Since C_{gs} is bias dependent, R_i is also bias dependent.

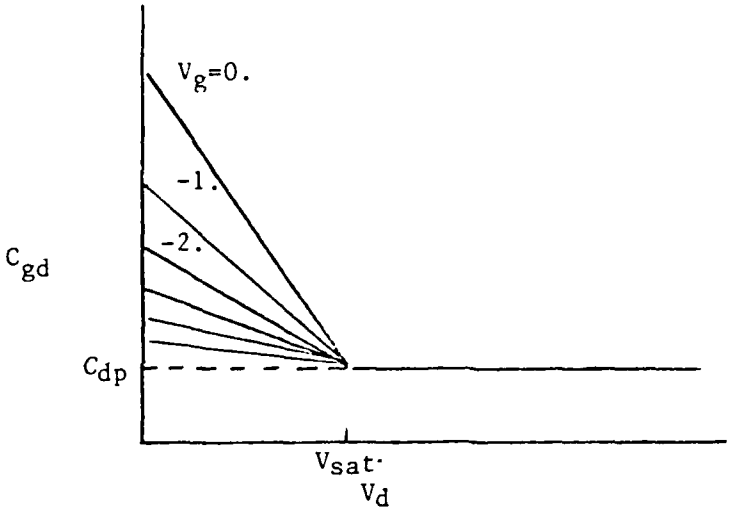


Figure 2.13 Voltage dependency of C_{gd}

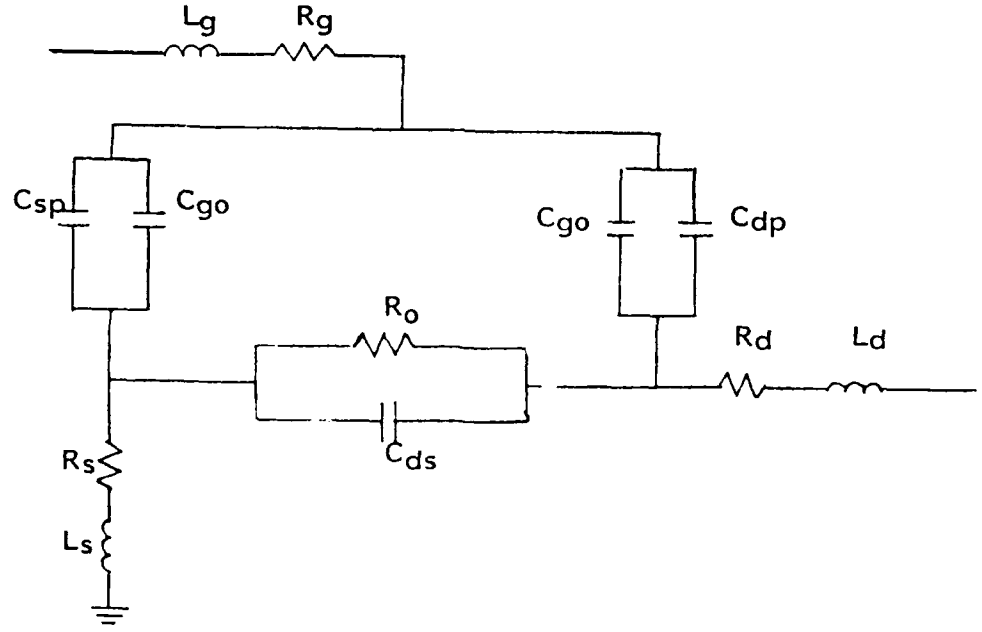


Figure 2.14 Zero biased equivalent circuit of MESFET

The magnitude of R_i is usually small. For simplicity, R_i is assumed constant in the model. The value of R_i can be optimized by using Super-Compact.

C_{ds} is the capacitance that exits in the channel region. Its value is expected to be small before saturation. After saturation, its value increases due to the formation of the Gunn domain dipole layer. For the PF-6000 MESFET, C_{ds} is found to be .2pf at zero biased condition(eg. V_{DS}=0., V_{GS}=0.) and is .4pf at V_{GS}=-2.V, V_{DS}=7.V. In this model a constant C_{ds} value is assumed. Willing, et al.[7], has stated this approximation is valid at least in the saturation region. The value of C_{ds} can be optimized at a bias point in the saturation region.

Chapter 3 Large Signal Analysis

3.1 Introduction

A nonlinear circuit analysis computer program is needed to simulate the large signal model. The multiple reflection method is chosen to analyze the nonlinear circuit. The advantage of this method over the popular harmonic balance method is in its reliable convergence nature and no initial guess requirement. The disadvantage is the longer computation time required. At the initial development stage of the MESFET model, reliability is certainly more important than efficiency of the simulation method. In this study, the multiple reflection method is improved by using an accelerated convergence scheme. This modified multiple reflection technique is found to be more efficient than the original one in this study.

In the multiple reflection algorithm and other hybrid time-frequency domain type methods, the circuit under analysis is divided into 2 parts: the FET intrinsic circuit and the external embedding circuit. The external embedding circuit consists of an input matching circuit and an output matching circuit. The intrinsic FET circuit is characterized by a set of nonlinear differential equations in the time domain. The external embedding circuit is conveniently represented by a set of linear phasor equations in the frequency domain. These 2 sets of equations must be solved simultaneously. In the harmonic balance method, the harmonic

compments of the voltage at the junctions of the FET circuit and external circuit are chosen as independent variables. These variables are optimized using iterative methods such as the steepest descents method and the Newton-Ralphson method. The solution is arrived at when the RMS difference of the currents at the junction, resulting from each set of equations are minimum. With a fast optimization routine, this harmonic balance approach can be quite efficient. However, there are two major problems with this approach. First of all, it requires an initial guess. The speed or even the success of this approach depends strongly on how good the initial guess is. Second, the optimization routine might converges to local minimums which makes the harmonic balance mehtod unreliable.

3.2 The Multiple reflection technique

In the multiple reflection technique, two ficticious transmission lines are assumed to exist between the intrinsic FET circuit and the input-output matching networks, as shown in fugure 3.1. The transmission lines are assumed lossless and are large integer multiples of wavelength long. With this assumption, the steady state solution is not changed by inserting these transmission lines.

At t=0, the gate and drain input voltages are applied to the transmission lines. The initial incident voltage wave to the FET circuit from the gate side is:

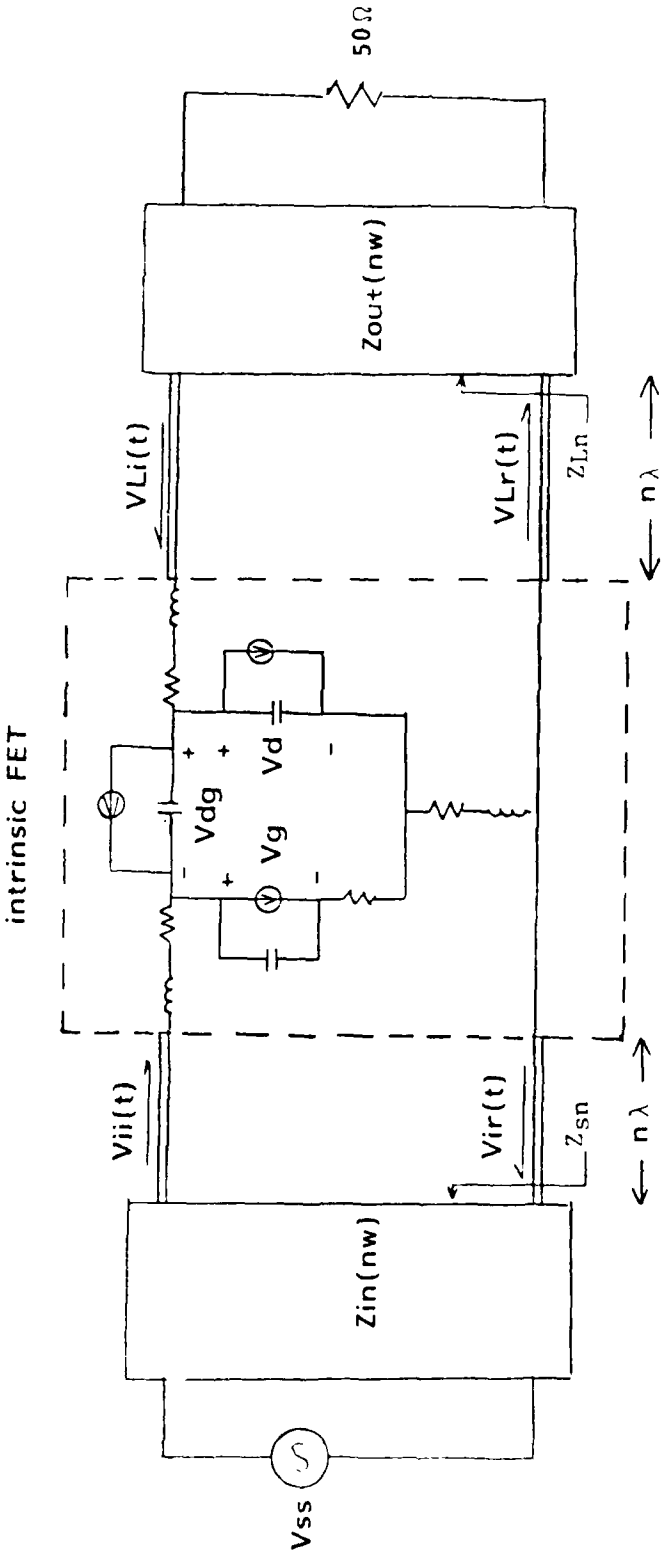


Fig.3.1 Schematic diagram of large signal analysis

$$V_{ii}^{1}(t)=V_{ss}\,Z_0/\mathrm{SQRT}(Z_0^2+Z_{s1}^2)\times\cos(\omega t-\mathrm{phase}) \qquad (3.1)$$

$$+V_{BB}\times Z_0/(Z_0+Z_{so})$$

$$,\ \text{where}\quad \mathrm{phase}=\tan^{-1}[\mathrm{Im}(Z_{s1})/(Z_0+\mathrm{Re}(Z_{s1}))]$$

The initial incident voltage from the drain side is

$$V_{Li}^{1}(t)=V_{DD}\times Z_0/(Z_0+Z_{Lo}) \qquad (3.2)$$

The superscript refers to the iteration number. These incident waves reach the FET, where the FET/transmission line interface can be described by the circuit of figure 3.2. This circuit is analyzed in time domain and will be discussed in next section. After the FET circuit reaches steady state, the reflected voltage waves are calculated as

$$V_{ir}^{1}(t)=V_{gs}^{1}(t)-I_g^{1}(t)\,Z_0$$

$$V_{Lr}^{1}(t)=V_{ds}^{1}(t)-I_d^{1}(t)\,Z_0 \qquad (3.3)$$

These voltage waves can be represented by Fourier series,

$$V_{ir}^{1}(t)=\sum_{n=0}^{\infty} V_{ir}^{1}(n\omega)\ e^{jn\omega t} \qquad (3.4)$$

$$V_{Lr}^{1}(t)=\sum_{n=0}^{\infty} V_{Lr}^{1}(n\omega)\ e^{jn\omega t}$$

Let the operation of calculating $V_{ir}(m\omega)$ and $V_{Lr}(m\omega)$ be $F_i[\ ]$ and $F_L[\ ]$ respectively, then

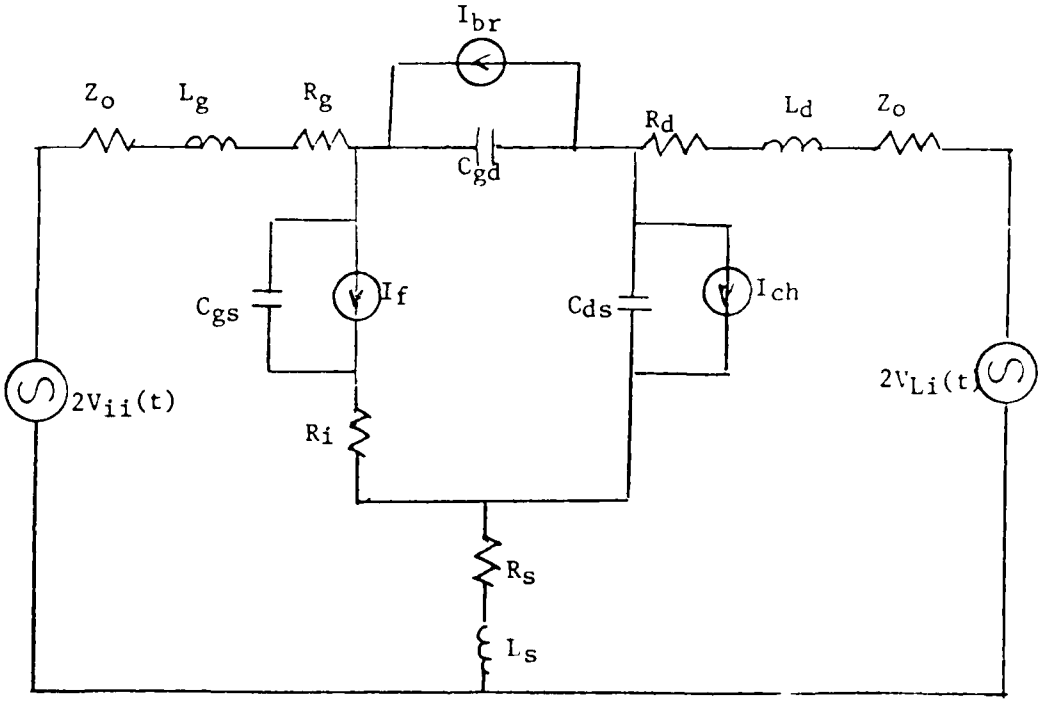


Figure 3.2 Equivalent circuit for FET/transmission line interface

$$V_{ir}(n\omega)=F_i[V_{ii}(t),V_{Li}(t)]$$

$$V_{Lr}(n\omega)=F_L[V_{ii}(t),V_{Li}(t)] \qquad (3.5)$$

$$n=0,1,2,\ldots$$

These reflected waves travel back to the embedding circuit and are reflected again.

The new incident waves are now equal to these reflected waves plus the initial incident waves

$$V_{ii}^{2}(t)=V_{ii}^{1}(t)+\sum_{n=1}^{\infty} V_{ir}^{1}(n\omega)\,\Gamma_i(n\omega)e^{jn\omega t} \qquad (3.6)$$

$$V_{Li}^{2}(t)=V_{Li}^{1}(t)+\sum_{n=1}^{\infty} V_{Lr}^{1}(n\omega)\,\Gamma_L(n\omega)e^{jn\omega t}$$

$\Gamma_i(n\omega)$ and $\Gamma_L(n\omega)$ are the reflection coefficients at the interfaces of the ficticious transmission lines and the input/output embedding circuits, respectively. $\Gamma_i(n\omega)$ and $\Gamma_L(n\omega)$ are calculated as

$$\Gamma_i(n\omega)=(Z_{sn}-Z_0)/(Z_{sn}+Z_0)$$

$$\Gamma_L(n\omega)=(Z_{Ln}-Z_0)/(Z_{Ln}+Z_0)$$

$$n=0,1,2,3,\ldots \qquad (3.7)$$

This process continues until the solution converges to a steady state value. The multiple reflection scheme is illustrated in figure 3.3. Convergence occurs when the RMS difference of the reflected waves on two consecutive iterations, is less than a tolerance value.

The value of the characteristic impedance of the ficticious transmission lines will affect the convergence speed. Z_0 should be chosen close to the value of Z_{s1} in order to minimize the reflection coefficient at the input end. Z_0 also affects the time for the intrinsic FET circuit to reach steady-state and therefore should not be too large. The values for characteristic impedance of the input transmission line and output transmission line need not be the same.

During iterations, the gate or drain voltage may exceed the limiting value of the model. This can be prevented by setting the DC source and load resistances to z_0, even though in practice they have small values. This change has no effect on the gate circuit because the gate current has a very small DC component. The DC voltage drop in the ficticious resistance can be compensated in the drain by offsetting the drain bias voltage.

3.3 Time domain analysis of the intrinsic FET circuit

During iterations, the circuit of figure 3.2 needs to be analyzed in the time domain. The inductance L_d and L_g are linear elements and can be moved outside the intrinsic FET circuit. Let

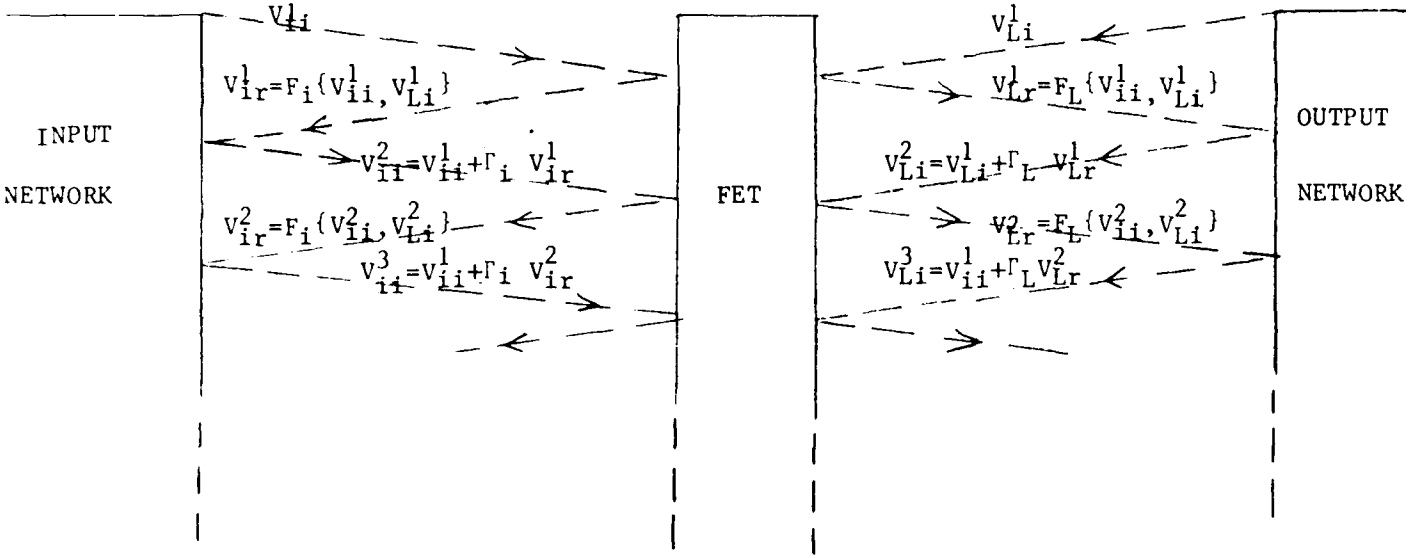


Figure 3.3 Multiple reflection scheme

$R_1=Z_0+R_g$ and $R_2=Z_0+R_d$ The circuit of figure 3.2 is written in the form of figure 3.4 To analyze the circuit of figure 3.4, 3 loops equations can be written

$$V_g(t)-V_p(t)-V_d(t)+R_i\, I_g(t)=0 \qquad (3.8)$$

$$-2V_{ii}(t)+(R_1+R_2)I_p(t)+V_p(t)+R_i\, I_g(t)-R_2\, I_d(t)+2V_{Li}(t)=0. \qquad (3.9)$$

$$2V_{ii}(t)+R_2 I_p(t)-R_s I_g(t)-(R_2+R_s)I_d(t)-V_d(t)-L_s(I_d(t)+Ig(t))=0. \qquad (3.10)$$

and three nonlinear equations can be written

$$I_g(t)=Cgs(V_g(t))\, V_g(t) + I_{so} \exp(\alpha\, V_g(t)) \qquad (3.11)$$

$$I_p(t)=C_{gd}(V_g(t),\, V_d(t))V_p(t)-I_{sr} \exp(-\beta\, V_p(t)) \qquad (3.12)$$

$$I_d(t)=I_{ch}(Vg(t-\tau),V_d(t))+C_{ds}\, V_d(t) \qquad (3.13)$$

These set of 6 equations can be solved by using numerical integration methods. The initial condition for voltages and currents of the first iteration are obtained by performing a DC analysis of the circuit. in other words, it is assumed DC voltages have been applied to the circuit for $t\leq 0$.

3.4 Modified multiple reflection technique

Hicks and Khan [23] proposed a voltage update algorithm to analyze nonlinear circuits. In this method the circuit under analysis is decomposed to two parts(figure 3.5). The linear portion

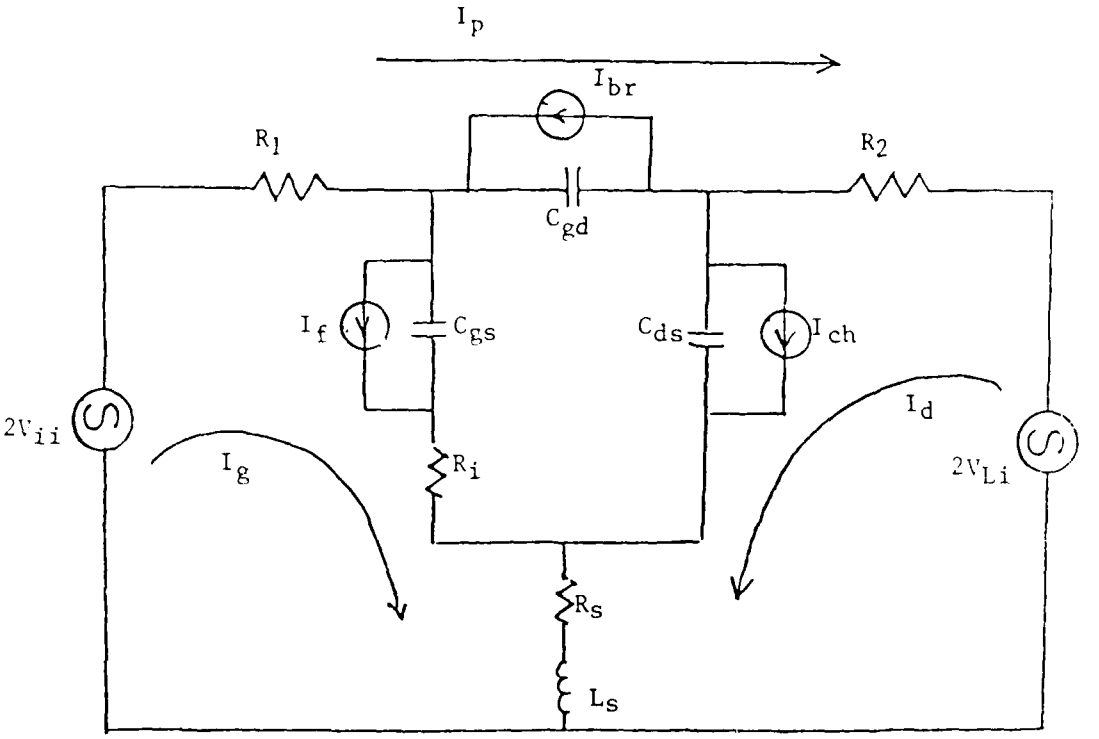


Figure 3.4 Intrinsic FET circuit analysis

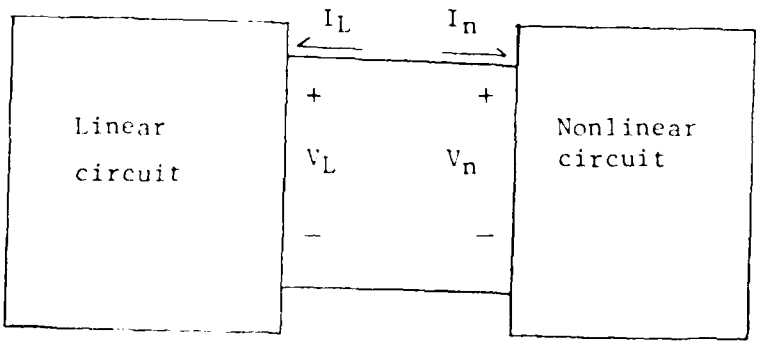


Figure 3.5 Schematic diagram of Hick & Khan's algorithm

and the nonlinear portion. The algorithm is described in the following steps.

1. Estimate the harmonic components of the periodic voltage at the interface $V_n^1(m\omega)$ (superscript indicated iteration number).

2. Apply $V_n^1(t)=\sum_{m=1}^{\infty} V_n^1(m\omega)e^{jm\omega t}$ to the nonlinear circuit, and calculate $I_n^1(t)$.

3. $I_L^1(t)=-I_n^1(t)$, take the Fourier transform of $I_L^1(t)$ to frequency domain.

4. Apply $I_L^1(m\omega)$ to the linear network and calculate $V_L^1(m\omega)$ for m=0,1,2. . . .

5. New harmonic components of the voltage applied to the nonlinear network are updated as,

$$V_n^{k+1}(m\omega)=V_n^k(m\omega)+P_m\,(V_L^k(m\omega)-V_n^k(m\omega)) \quad ,0<P_m\leq 1 \qquad (3.14)$$

The process continues until the RMS difference of $V_n(t)$ and $V_L(t)$ is less than a specified tolerance value.

A similar voltage update scheme can be used to improve the multiple reflection technique. Let $F_i[v_{ii}(t),V_{Li}(t)]$ and $F_L[V_{ii}(t),V_{Li}(t)]$ be the reflected voltage waves at the input and output terminals respectively in the original multiple reflection

algorithm (as defined in section 3.2). Using the voltage update scheme

$$V_{ir}^{k}(m\omega)=V_{ir}^{k-1}(m\omega)+p_m(F_i[V_{ii}^{k}(t),V_{Li}^{k}(t)]-V_{ir}^{k-1}(m\omega)) \quad (3.15)$$

$$V_{Lr}^{k}(m\omega)=V_{Lr}^{k-1}(m\omega)+p_m(F_L[V_{ii}^{k}(t),V_{Li}^{k}(t)]-V_{Lr}^{K-1}(m\omega))$$

$$0.<P_m\leq 1., \; m=0,1,2,3,\ldots$$

with this modification, the speed of convergence can be increased significantly. The values of P_m affect the speed of convergence. The multiple reflection technique is the limiting case of this algorithm with $P_m=1$. Typically, the optimum values of Pm is .5 for MESFET analysis.

Chapter 4 Results

The validity of the large signal model is confirmed in two ways. First, a small signal equivalent circuit at an arbitrary bias point can be derived from the large signal model. The S-parameters of this small signal equivalent circuit are calculated and compared with the measured S-parameters(supplied by Hughes Air Craft) of the device at that bias point. Second, the large signal model is simulated in an amplifier confuguration. The power input versus power output curve is simulated and is compared with measured data(supplied by Hughes Air Craft). Using the methods in chapter 2, the circuit elements and parameters are obtained and are listed in table 4.1.

4.1 S-Parameters comparison

The parameters G_m and R_0 in the small signal equivalent circuit(figure 2.1) can be derived from the large signal model at a bias condition.

$$G_m = \frac{\partial I_{ch}(Vg,Vd)}{\partial Vg}\bigg|_{V_{GG},V_{DD}} \qquad (4.1)$$

$$R_0 = \frac{\partial Ich(Vg,Vd)}{\partial Vd}\bigg|_{V_{GG},V_{DD}}$$

where V_{GG} and V_{DD} are the gate and drain bias voltages,respectively. From the linear element values in table 4.1 and G_m , R_0 as derived, the S-parameters of this equivalent circuit can be calculated conveniently using Super-Compact. The S-parameters thus calculated for the PF-6000 MESFET are shown in figure 4.1 along with the measured S-parameters of the device at V_{GG}=-2.03V, V_{DD}=7.V.

4.2 Large signal simulation

The validity of the modified multiple reflection method is first verified by comparing it with the MESFET simulation results of Materka and Kacprzak [10]. The circuit parameters of Materka's amplifier are given in table 4.2. The model is simulated in an amplifier configuration as shown in figure 4.2. The termination impedances are given in table 4.3. The results are shown in figure 4.3. By means of the modified multiple reflection method, the solution to this particular simulation usually coverges within 5 iterations. When the original multiple reflection method was used, the soultions converged after 18 iterations.

The model of PF-6000 MESFET is also simulated in the amplifier configuration. The input has a 50 ohm termination and the output has a 11+8.5j termination impedance at 15 GHZ. Figure 4.4 shows the simulated and measured output power versus input power curves. The simulation takes an average of 7 iterations to converge with the modified multiple reflection method. When the original

Table 4.1

Model parameters for Hughes' PF-6000 MESFET

R_s	.75 Ω	C_{ds}	.4pf	g_o	.279	I_{sr}	.13mA
R_d	.80Ω	C_{sp}	.079pf	q	2.56	β	.231
R_g	1.14Ω	C_{so}	.613pf	V_{po}	-5.28v	I_{so}	1.05 pA
R_i	.65 Ω	C_{go}	.645pf	γ	-.227	α	34
L_s	.012nH	C_{dp}	.079pf	V_s	2.23		
L_d	.092nH	I_{dss}	496mA	V_{sat}	1.85		
L_g	.127nH	c	4.52	τ	4.7ps		

Table 4.2

Model parameters for Materka's MESFET

R_s	4.5Ω	C_{ds}	.1pf	g_o	----	I_{sr}	.65nA
R_d	4.5Ω	C_{sp}	---	q	-----	β	1.28
R_g	4.5Ω	C_{so}	.64pf	V_{po}	-1.78v	I_{so}	1.45nA
R_i	10.Ω	C_{go}	----	g	-.11	α	23
L_s	.1nH	C_{dp}	.026pf	V_s	-----		
L_d	.2nH	I_{dss}	75mA	V_{sat}	-----		
L_g	.2nH	c	3.35	τ	5.ps		

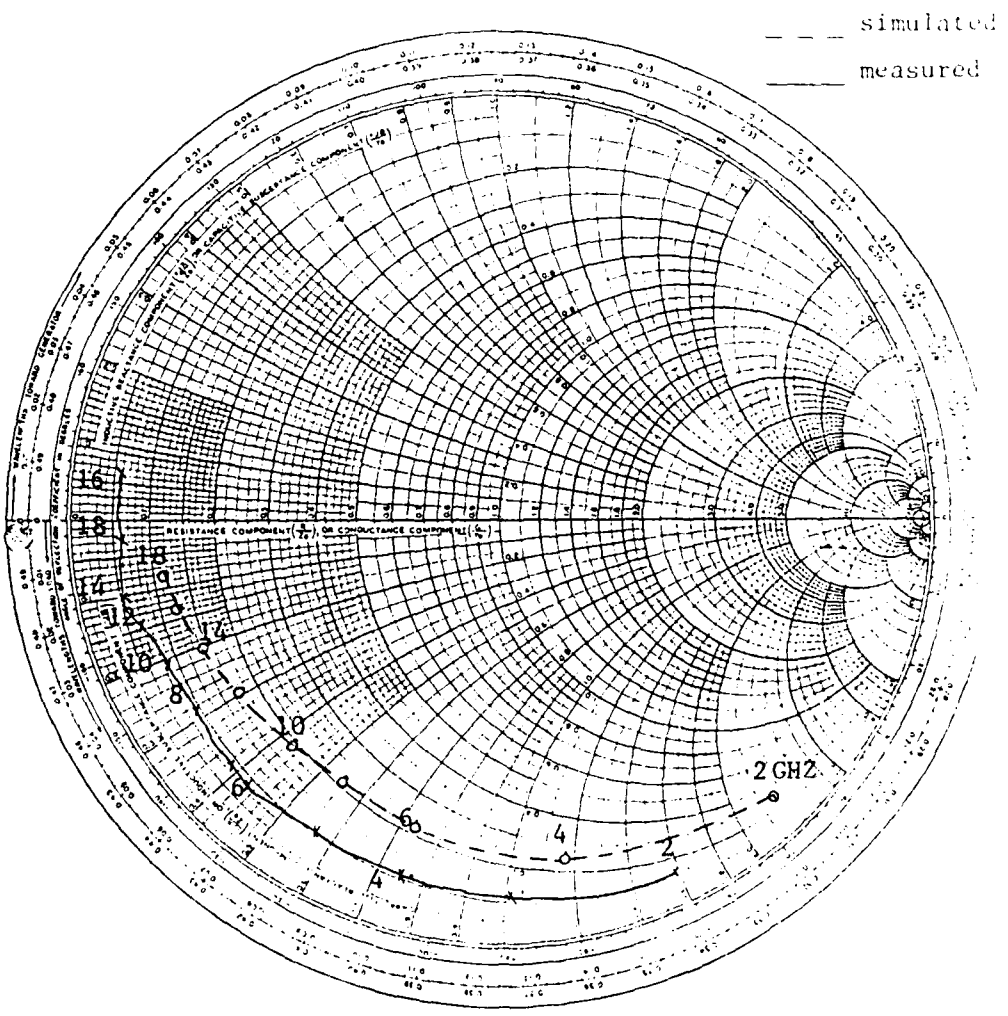


Figure 4.1a Measured and simulated S_{11} of PF-6000 MESFET

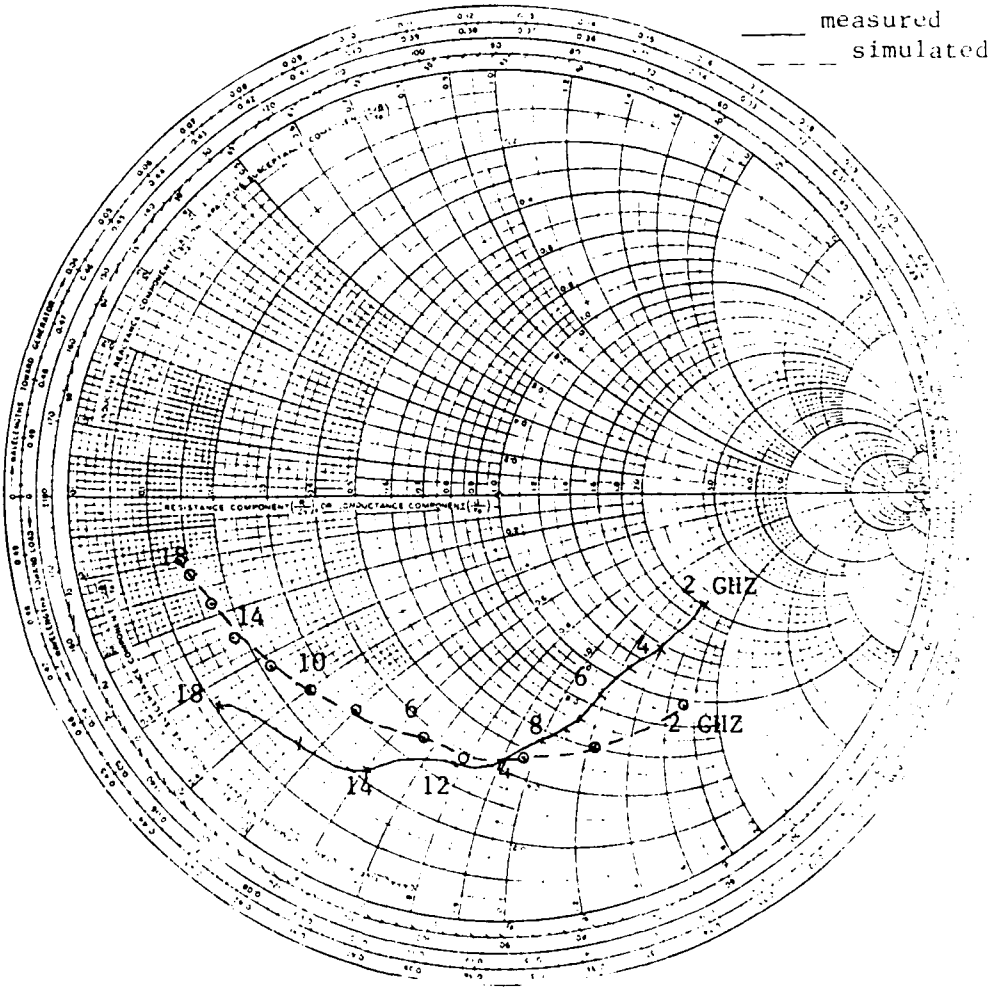


Figure 4.1b Measured and simulated S_{22} of PF-6000 MESFET

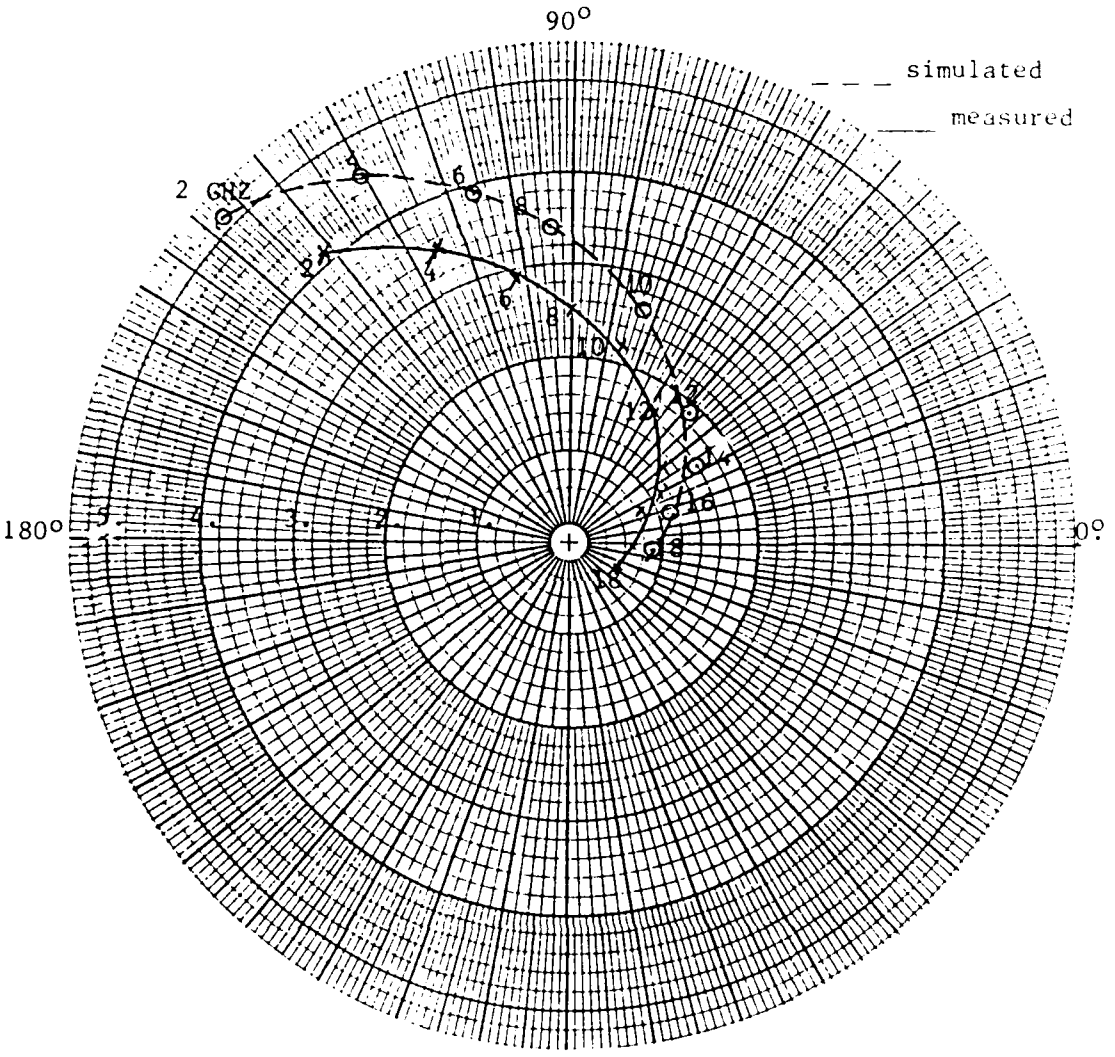


Figure 4.1c Measured and simulated S_{21} of PF-6000 MESFET

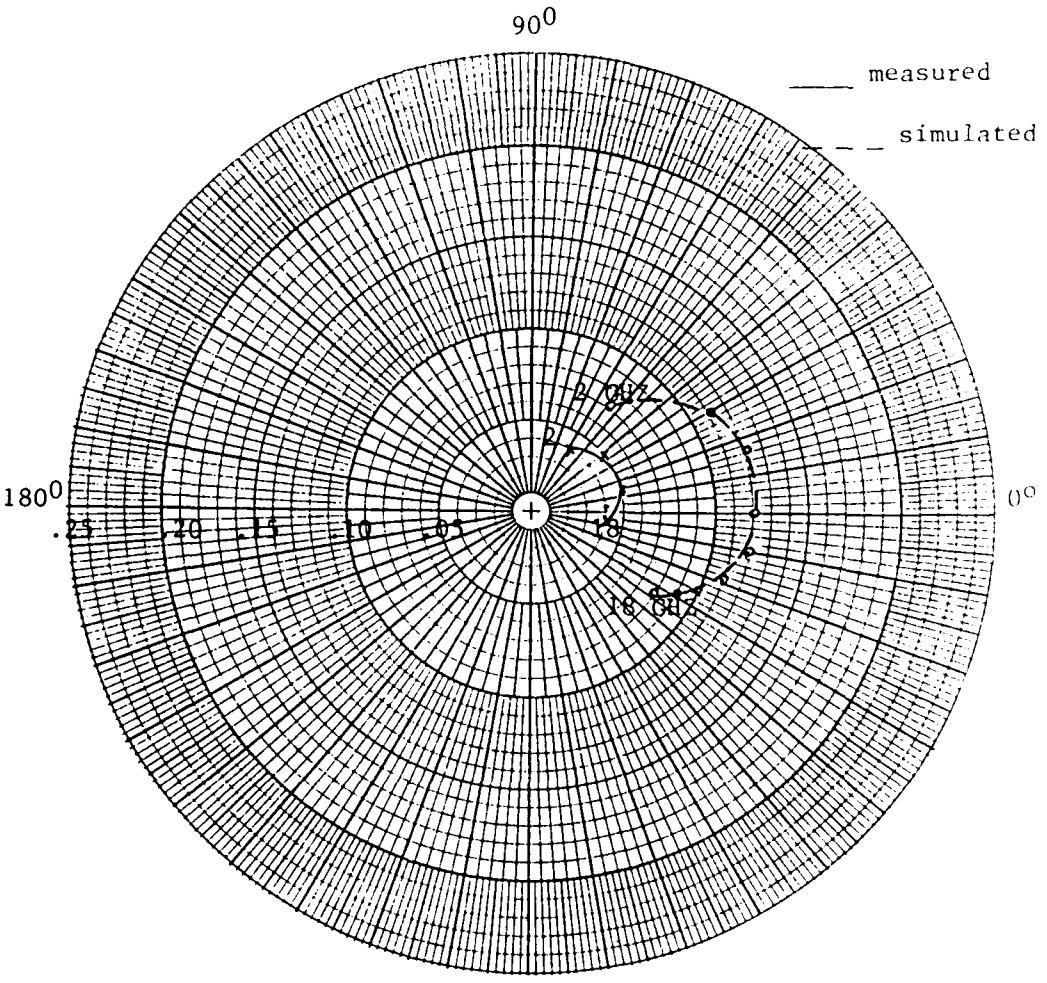


Figure 4.1d Measured and simulated S_{12} of PF-6000 MESFET

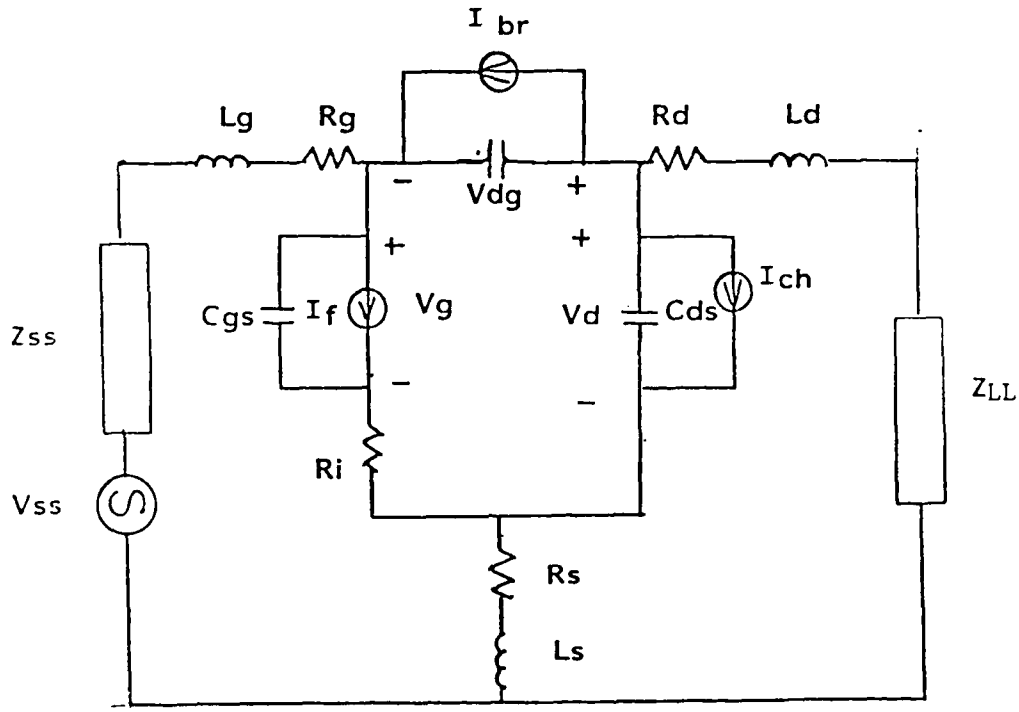


Fig.4.2 Simplified amplifier configuration.

Table 4.3

Termination impedances for Materka's amplifier simulation

	V_{GS}=-.75v		V_{GS}=-1.25v	
Pi(mw)	Z_{SS}	Z_{LL}	Z_{SS}	Z_{LL}
5.	16.8+32.3j	67.9+67.6j	24.9+15.8j	55.0+85.9j
10.	18.4+33.1j	62.7+41.9j	38.8+17.7j	67.6+62.7j
15.	19.3+32.7j	60.2+27.3j	48.3+18.7j	68.9+45.6j
20.	19.8+32.5j	55.8+19.8j	55.8+19.1j	64.9+35.2j
25.	20.0+31.7j	53.6+16.1j	62.1+19.4j	61.1+27.0j
30.	20.2+31.4j	49.3+13.0j	67.5+19.6j	57.9+22.7j
35.	21.4+31.5j	47.2+11.3j	72.2+19.7j	56.4+18.0j
40	23.0+30.9j	47.5+10.5j	76.1+19.6j	54.1+14.9j

Table 4.3a V_{DS}=4.V

	V_{DS}=3.0V		V_{DS}=5.0V	
P_i(mw)	Z_{SS}	Z_{LL}	Z_{SS}	Z_{LL}
5.	18.6+32.8j	68.1+44.3j	15.8+31.8j	59.0+84.8j
10.	19.3+33.6j	54.4+24.5j	18.4+32.0j	68.4+62.7j
15.	19.9+33.3j	47.6+14.5j	19.7+32.3j	70.8+42.7j
20.	20.3+32.8j	44.2+ 9.6j	20.1+32.4j	64.0+32.3j
25.	20.3+31.2j	42.3+ 9.1j	20.6+31.8j	62.0+26.6j
30.	20.9+31.3j	41.4+ 5.9j	20.7+31.1j	60.0+20.7j
35.	22.3+30.8j	41.0+ 5.2j	21.5+30.6j	59.3+16.8j
40.	23.9+40.7j	40.7+ 4.9j	22.7+30.2j	59.1+15.8j

Table 4.3b V_{GS}=-.75V

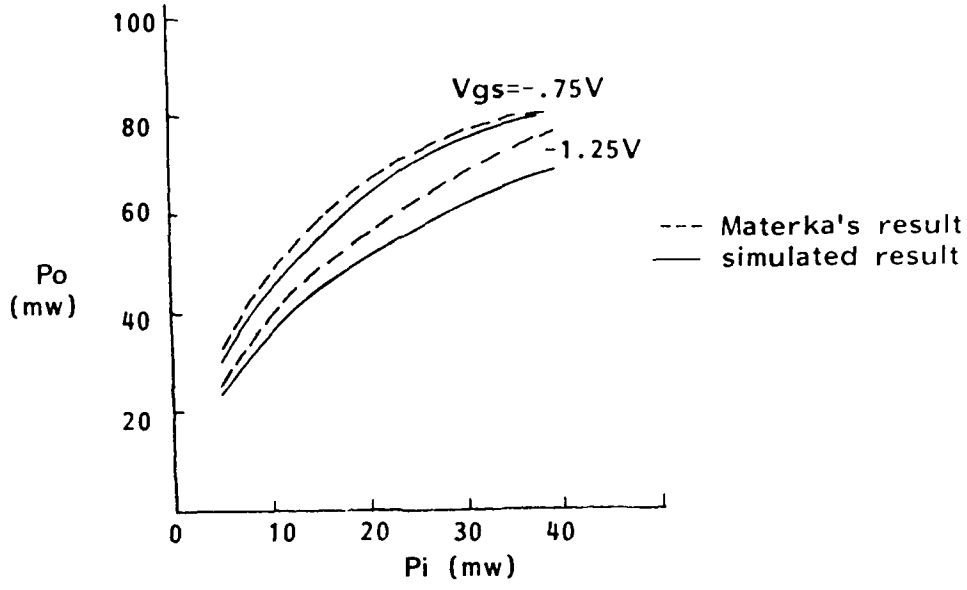


Fig 4.3a Output power vs. input power of Materka's amplifier, f=9.5 GHz, Vds=4V.

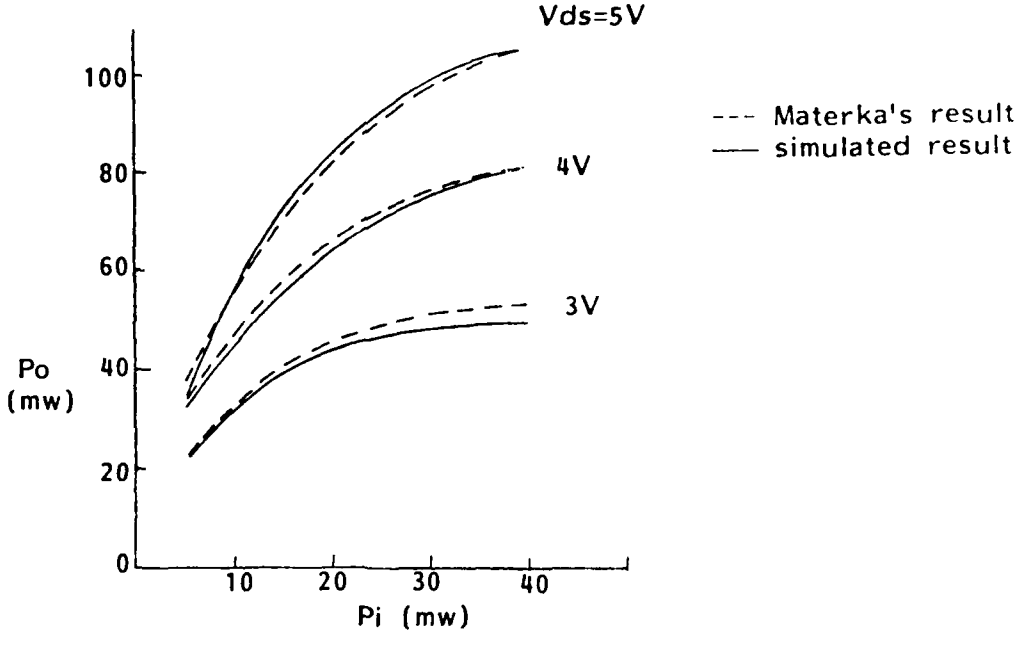


Fig.4.3b Output vs. input power of Materka's amplifier, f=9.5 GHz, Vgs=-.75V

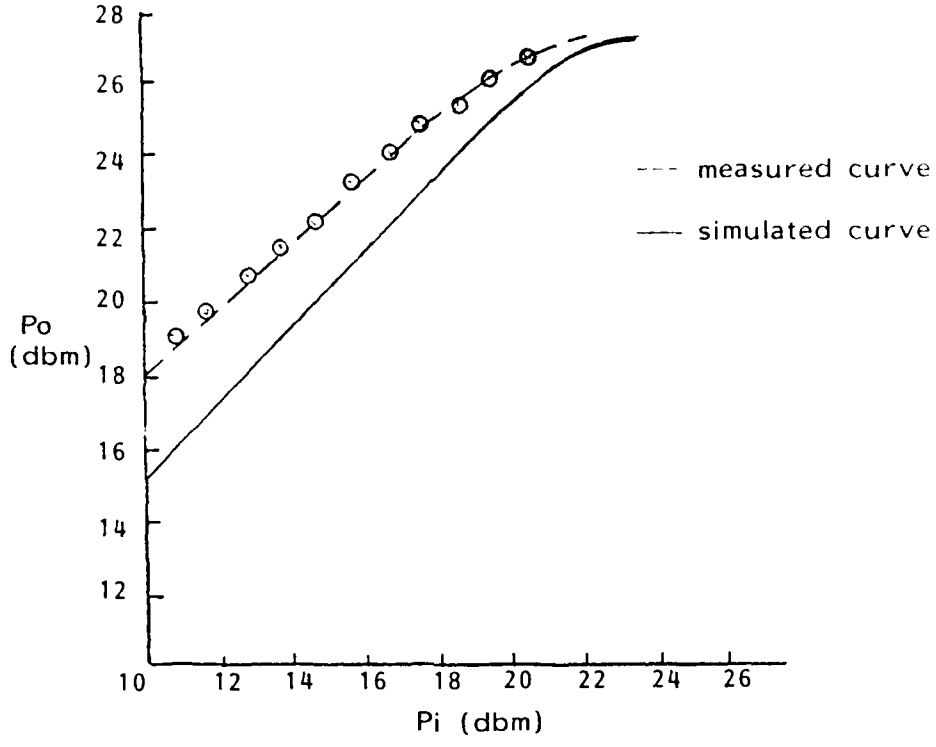


Fig.4.4 Output power vs. input power curve of PF-6000 MESFET, VDS=7V, VGS=-2.03V, f=15GHz, Zss=50Ω, ZLL=11+8.5j.

multiple reflection method was used, the solution still does not converge after 50 iterations, even for a small input power.

When simulating the circuit of Materka and Kacprzak, the termination impedances are matched to the FET. Multiple reflection method works fairly well when termination impedances are matched. In the second case, the input termination to the PF-6000 MESFET is 50 ohm and is mismatched. the multiple reflection method runs into a convergence problem. The modified multiple reflection method shows good covergence speed in both cases.

Chapter 5 Conclusion and suggestion for further research

The modeling method in chapter 2 is shown to be effective, yet relatively simple to implement. This approach is very general; it can be applied to MESFETs with various dimensions and physical parameters. A powerful computer aided design system can be developed by automating the circuit element and parameter extracting procedures and linking then together with Super-Compact and the curcuit sumulator.

The modified multiple reflection method is shown to be efficient. The accuracy of this method is confirmed by comparing its results with the experimental data and the simulated data of Materka *and Kacprzak*. The validity of the large signal model is confirmed by comparing the simulated and measured output power versus input power curves of the PF-6000 MESFET. On the average, there is about 3 dBm difference between the measured data and sumulated results. This difference is expected to be contributed by 3 factors:

1. Inadequacy of the model.
2. Errors involved in circuit parameter and element extracting procedures.
3. Errors in output power versus input power measurements and in load impedance measurements.

As stated in chapter 2, every circuit element of the model exhibits some degree of nonlinearity in practice. In the present model, the

drain to sourch capacitance C_{ds} is considered as linear element. To improve the accuracy, C_{ds} probably should be modeled as a nonlinear element. C_{ds} constitutes the capacitance due to the drain and source electrodes and the capacitance due to the Gunn domain dipole. The Gunn domain capacitance is certainly voltage dependent in nature.

5.2 Suggestion for further research

Several areas of further research related to this topic can be suggested. In the theoretical arena, the Gunn domain phenomenon of the GaAs MESFET needs to be investigated. This Gunn domain effect is expected to be one of the limitations of the GaAs MESFET. Shur[5] and Sing[6] have developed an analytical model for the Gunn domain. However, their model has not been validated under large-signal condition.

Using the large signal model developed for the GaAs MESFET, other microwave devices containing this MESFET can be analyzed. The modified multiple reflection technique can be applied directly to MESFET multiplier analysis. For MESFET mixer analysis, a two steps large-signal local oscillator, small-signal RF signal approach taken. The multiple reflection mehtod can be used to analyze the large signal MESFET curcuit with a local oscillator input power. A subsequent small-signal analysis is needed to calculate the RF-IF signal coversion characteristic of the mixer.

For MESFET oscillator simulation, the harmonic balance

method is the more appropriate technique to use. This is due to the fact that the oscillating frequency and the termination impedances can be taken as variables to be optimized. The optimization algorithm proposed by Walt[24] for diode analysis is shown to be very fast and efficient. Thus, this algorithm can be exploited for oscillator analysis.

Another interesting topic is the modeling and simulation of a dual-gate MESFET. Dual-gate MESFET can be utilized in mixer design in which the local oscillator signal and the RF signal are applied separately to the two different gates. This results in a simpler design of a mixer circuit. The dual gate MESFET can also be used for a self-oscilating mixer in which one of the gate is terminated by variable short or open circuit to produce local oscillator power.

Reference

[1] K. Yamaguchi, S. Asai and K. Kodera, "Two-dimensional numerical analysis of Stability creteria of GaAs FETs," IEEE Trans. Electron Devices, vol. ED-23, pp. 1283-1290, Dec. 1976.

[2] W.R. Curtice, Y. Yun, "A temprature model for the GaAs MESFET," IEEE Trans. Electron Devices, vol. ED-28, pp. 954-962, 1981.

[3] N. H. Song, T. Itoh, "Accurate simulation of MESFET by finite element method including energy transport and substrate effects," 1985 European Microwave Conference, pp. 245-250.

[4] A. Madjar and F.J. Rosenbaum, "Analysis of a microwave FET oscillator using an efficient computer model for the device," IEEE Trans. Microwave Theory and Tech., vol. MTT-30, pp.915-917, June 1982.

[5] M. S. Shur, "Analytical model of GaAs MESFETs," IEEE Trans. Electron Devices, vol. ED-25, pp. 612-618, June 1978.

[6] L.O. Chua and Y.W. Sing, "Nonlinear lumped curcuit moodel of GaAs MESFET," IEEE Trans. Electron Devices, vol. ED-30, pp. 825-833, July 1983.

[7] H. A. Willing, C. Rausher and P. de Santis, "A technique for predicting large-signal performance of a GaAs MESFET," IEEE Trans. Microwave Theory and Tech., vol. MTT-26, pp. 1017-1023, Dec. 1978.

[8] Y. Tajima, B. Wrona and K. Mishima, "GaAs FET large signal model and its application to circuit design," IEEE Trans Electron

Devices, ED-28, pp. 171-175, Feb. 1981.

[9] Y. Tajima nad Patrick d. Miller, "Design of broad band power GaAs FET amplifier," IEEE Trans. Microwave Theory and Tech., vol. MTT-32, Mar. 1984.

[10] A. Materka and T. Kacprzak, "Compter calculation of large-signal GaAs FET amplifier characteristics," IEEE Trans Microwave Theory and Tech., vol. MTT-33, pp. 129-134, Feb. 1985.

[11] F.R. Colon and T. N. Trick, "Fast periodic steady-state analysis for large-signal electronic circuit," IEEF Journal of solid-State Circuits, vol. SC-8, Aug. 1973.

[12] S. Skelboe, "Computation of the periodic steady-state response of nonlinear networks by extrapolation methods," IEEE trans. on Circuits and Systems, vol. CAS-27, Mar. 1980.

[13] M. Nakhla and J. Vlach, "A piecewise harmonic balance technique for determination of periodic response of nonlinear systems," IEEE Trans. on Circuit and System, vol. CAS-23, Feb. 1976.

[14] D.N. Held and A.R. Kerr, "Conversion loss and noise of microwave and millimeter wave mixer," IEEE Trans. Microwave Theory and Tech., vol. MTT-26, pp. 49-54, Feb. 1978.

[15] F. Diamond and M. Laviron, "Measurement of athe extrinsic series elements of a microwave MESFET under zero current condition," Proc. of 12th European Microwave Conf., Sept. 1982.

[16] W.R. Curtice and L. Camisa, "Self-consistant GaAs models for amplifier design and device diagonostics," IEEE Trans on

Microwave Theory and Tech., vol. MTT-32, Dec. 1984.

[17] H. Fukui, "Determinations of the basic parameters of a GaAs MESFET," Bell Syst. Tech. J., vol.-S8, Mar. 1979.

[18] Super-Compact, Linear Circuit Analysis and Optimization, Compact Engineering, Palo Alto, CA, 1981.

[19] C. Moglestue, "Negative differential resistivity in field-effect transistors," IEE Proceedings, vol. 130, Dec. 1983.

[20] J. Ruch, "Electron dynamics in short channel field-effect transistors," IEEE Trans. Electron Devices, vol. ED-19, May 1972.

[21] K. C. Gupta, et al., " Microstrip lines and slot lines," Artech House Inc., Dedham, Massachusetts, 1981.

[22] S.A. Mass, "Theory and analysis of GaAs MESFET mixers," IEEE Trans. on microwave Theory and Tech., vol. MTT-32, Oct. 1984.

[23] R.G. Hicks and P.J. Khan, "Numerical technique for determining pumped nonlinear device waveforms," Electronics letters, vol. 16, May 1980.

[24] P.W. Van Der Walt, "Efficient technuque for solving nonlinear mixer pumping problem," IEE Electronic Letters, vol. 21, Sept. 1985.

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